AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A power model for ~~a semiconductor~~ an integrated circuit,

wherein said power model comprises a logic gate circuit part representing an operating part of said ~~semiconductor~~ integrated circuit and an equivalent internal capacitive part representing a non-operating part of said ~~semiconductor~~ integrated circuit.

2. (currently amended) The power model as claimed in claim 1, wherein said power model is independently provided for each of plural power systems which are independent from each other and included in said ~~semiconductor~~ integrated circuit.

3. (currently amended) The power model as claimed in claim 1, wherein an internal circuit ~~configurations~~ configuration of said ~~semiconductor~~ integrated circuit ~~are~~ is divided into plural blocks on the basis of arrangement ~~informations~~ information, and a separate said power model is provided for each of said plural blocks.

4. (currently amended) The power model as claimed in claim 1, wherein an internal circuit ~~configurations~~ configuration of said semiconductor integrated circuit ~~are~~ is divided into plural groups, wherein each of said plural groups comprises ~~a~~

~~same timing group which includes~~ logic gate circuits having ~~individual~~ signal transmission delay times ~~fallen~~ in a ~~group-belonging~~ predetermined time range which ~~belongs to~~ is different for each of said plural groups, and wherein a separate said power model is provided for each of said plural groups.

5. (currently amended) The power model as claimed in claim 1, wherein said power model further comprises a signal source connected to said logic gate circuit part for supplying a frequency-fixed signal to said logic gate circuit part, so that said logic gate circuit part represents operating state parts of said ~~semiconductor~~ integrated circuit in accordance with said frequency-fixed signal, and said equivalent internal capacitive part represents non-operating state parts of said ~~semiconductor~~ integrated circuit.

6. (currently amended) The power model as claimed in claim 5, wherein said equivalent internal capacitive part further represents operating-irrelevant fixed parts of said ~~semiconductor~~ integrated circuit.

7. (currently amended) The power model as claimed in claim 6, wherein said logic gate circuit part is connected between first and second ~~powers~~ power terminals, and said equivalent internal capacitive part is also connected between said first and second ~~powers~~ power terminals.

8. (currently amended) The power model as claimed in claim 7, wherein said logic gate circuit part further comprises a single pair of an inverter circuit and a load capacitive element,

and said inverter circuit is connected between said first and second ~~powers~~ power terminals and said load capacitive element is also connected between said first and second ~~powers~~ power terminals, and said load capacitive element is placed between said inverter circuit and said equivalent internal capacitive part.

9. (currently amended) The power model as claimed in claim 8, wherein said load capacitive element comprises a series connection of a first load capacitance and a second load capacitance between said first and second ~~powers~~ power terminals, and an intermediate point between said first and second load capacitances is connected to an output terminal of said inverter circuit.

10. (currently amended) The power model as claimed in claim 9, wherein said equivalent internal capacitive part further comprises at least an equivalent internal capacitive element connected between said first and second ~~powers~~ power terminals.

11. (currently amended) The power model as claimed in claim 10, wherein a plurality of said equivalent internal capacitive element is connected between said first and second ~~powers~~ power terminals, and said equivalent internal capacitive element comprises a series connection of a capacitance and a resistance between said first and second ~~powers~~ power terminals.

12. (original) The power model as claimed in claim 11, wherein said inverter circuit comprises a series connection of a p-channel MOS field effect transistor and an n-channel MOS field

effect transistor, and gate electrodes of said p-channel and n-channel MOS field effect transistors are connected to a clock signal source for applying a clock signal to said gate electrodes of said p-channel and n-channel MOS field effect transistors.

13. (currently amended) The power model as claimed in claim 7, wherein said logic gate circuit part further comprises plural pairs of an inverter circuit and a load capacitive element, and said inverter circuit is connected between said first and second ~~powers~~ power terminals and said load capacitive element is also connected between said first and second ~~powers~~ power terminals, and in each pair, said load capacitive element is placed closer to said equivalent internal capacitive part than said inverter circuit.

14. (currently amended) The power model as claimed in claim 13, wherein said load capacitive element comprises a series connection of a first load capacitance and a second load capacitance between said first and second ~~powers~~ power terminals, and an intermediate point between said first and second load capacitances is connected to an output terminal of said inverter circuit.

15. (currently amended) The power model as claimed in claim 14, wherein said equivalent internal capacitive part further comprises at least an equivalent internal capacitive element connected between said first and second ~~powers~~ power terminals.

16. (currently amended) The power model as claimed in claim 15, wherein a plurality of said equivalent internal capacitive element is connected between said first and second ~~powers~~ power terminals, and said equivalent internal capacitive element comprises a series connection of a capacitance and a resistance between said first and second ~~powers~~ power terminals.

17. (original) The power model as claimed in claim 16, wherein said inverter circuit comprises a series connection of a p-channel MOS field effect transistor and an n-channel MOS field effect transistor, and gate electrodes of said p-channel and n-channel MOS field effect transistors are connected to a clock signal source for applying a clock signal to said gate electrodes of said p-channel and n-channel MOS field effect transistors.

18. (original) The power model as claimed in claim 1, wherein said equivalent internal capacitive part is placed between said logic gate circuit part and a power system side.

19. (currently amended) The power model as claimed in claim 1, wherein said power model ~~is deigned for simulation to~~ simulates a current distribution over a circuit board on which said ~~semiconductor~~ integrated circuit is mounted.

20. (currently amended) The power model as claimed in claim 19, wherein said power model ~~is deigned for an~~ simulates electro-magnetic interference ~~simulation to an electromagnetic field distribution~~ over a circuit board on which said ~~semiconductor~~ integrated circuit is mounted.

21. (currently amended) A method of designing a power model for ~~a semiconductor~~ an integrated circuit, and said power model comprising a logic gate circuit part and an equivalent internal capacitive part, the method comprising the steps of:

~~wherein~~ performing first sequential processes to prepare said logic gate circuit part of said power model taking into account operating-related ~~informations~~ information of all gate circuits constituting said ~~semiconductor~~ integrated circuit ~~are utilized in first sequential processes to prepare said logic gate circuit part of said power model~~, and

~~wherein~~ performing second sequential processes separate from said first sequential processes to prepare said equivalent internal capacitive part of said power model taking into account non-operating-related ~~informations~~ information of said all gate circuits constituting said ~~semiconductor~~ integrated circuit ~~are utilized in second sequential processes separated from said first sequential processes to prepare said equivalent internal capacitive part of said power model~~.

22. (currently amended) The method as claimed in claim 21, wherein, in said first sequential processes, ~~informations~~ information about gate widths of operating-state p-channel transistors in said operating-state of said constituting gate circuits ~~are utilized to decide~~ determines a gate width of a model p-channel transistor;

~~informations~~ information about gate widths of operating-state n-channel transistors in said operating-state of

said constituting gate circuits ~~are utilized to decide~~ determines a gate width of a model n-channel transistor;

~~informations~~ information about gate ~~capacities~~ capacitances of said operating-state p-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state p-channel transistors and a first power ~~are utilized to decide~~ terminal determines a model first load ~~capacity~~ capacitance; [[and]]

~~informations~~ information about gate ~~capacities~~ capacitances of said operating-state n-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state n-channel transistors and a second power ~~are utilized to decide~~ terminal determines a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with at least a pair of p-channel and n-channel transistors and at least a pair of first and second load ~~capacities is designed~~ capacitances.

23. (currently amended) The method as claimed in claim 22, wherein a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity; and~~ capacitance;

a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

24. (currently amended) The method as claimed in claim 22, wherein a half of a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting

gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity; and~~ capacitance;

a half of a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

25. (currently amended) The method as claimed in claim 22, wherein a product of the number of said operating-state gate circuits and an ~~averaged~~ average value of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said operating-state gate circuits and an ~~averaged~~ average value of gate widths of operating-state n-channel transistors in said operating-state of

said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

26. (currently amended) The method as claimed in claim 22, wherein a half of a product of the number of said operating-state gate circuits and an ~~averaged~~ average value of gate widths of said operating-state p-channel transistors in said operating-

state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said operating-state gate circuits and an ~~averaged~~ average value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

27. (currently amended) The method as claimed in claim 21, wherein, in said first sequential processes, ~~informations~~ information about gate widths of all p-channel transistors of said constituting gate circuits and [[an]] information about operational rate of operating-state p-channel transistors in said operating-state ~~are utilized to decide~~ determine a gate width of a model p-channel transistor;

~~informations~~ information about gate widths of all n-channel transistors of said constituting gate circuits and [[an]] information about operational rate of operating-state n-channel transistors in said operating-state ~~are utilized to decide~~ determine a gate width of a model n-channel transistor;

~~informations~~ information about gate ~~capacities~~ capacitances of said all p-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all p-channel transistors and a first power terminal and ~~informations~~ information about said operational rate ~~are utilized to decide~~ determine a model first load ~~capacity ; and~~ capacitance;

~~informations~~ information about gate ~~capacities~~ capacitances of said all n-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all n-channel transistors and a second power terminal and ~~informations~~ information about said operational rate ~~are utilized to decide~~ determine a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with at least a pair of said model p-channel and n-channel transistors and at least a pair of said model first and second load ~~capacities is designed~~ capacitances.

28. (currently amended) The method as claimed in claim 27, wherein a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all

n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

29. (currently amended) The method as claimed in claim 27, wherein a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel

transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

30. (currently amended) The method as claimed in claim 27, wherein a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both

a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

31. (currently amended) The method as claimed in claim 27, wherein a half of a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel

transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

32. (currently amended) The method as claimed in claim 21, wherein, in said first sequential processes, ~~informations~~ information about gate widths of all p-channel transistors of said constituting gate circuits and ~~informations~~ information about currents of basic gate circuits and said constituting gate

circuits ~~are utilized to decide~~ determine a gate width of a model p-channel transistor;

~~informations~~ information about gate widths of all n-channel transistors of said constituting gate circuits and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine a gate width of a model n-channel transistor;

~~informations~~ information about gate ~~capacities~~ capacitances of said all p-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all p-channel transistors and a first power terminal and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine a model first load ~~capacity ; and~~ capacitance;

~~informations~~ information about gate ~~capacities~~ capacitances of said all n-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all n-channel transistors and a second power terminal and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with at least a pair of p-

channel and n-channel transistors and at least a pair of first and second load ~~capacities is designed~~ capacitances.

33. (currently amended) The method as claimed in claim 32, wherein a product of the number of said all gate circuits, and a power current ratio of an ~~averaged~~ average current value of said basic gate circuits to an ~~averaged~~ average current value of said constituting gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said all gate circuits, said power current ratio, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances

between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

34. (currently amended) The method as claimed in claim 32, wherein a half of a product of the number of said all gate circuits, and a power current ratio of an ~~averaged~~ average current value of said basic gate circuits to an ~~averaged~~ average current value of said constituting gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said all gate circuits, said power current ratio, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel

transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

35. (currently amended) The method as claimed in claim 21, wherein, in said second sequential processes, ~~informations~~ information about ON-resistances of non-operating-state transistors in said non-operating-state of said constituting gate circuits ~~are utilized to decide~~ determines an ON-resistance of an equivalent internal ~~capacity ; and~~ capacitance;

~~informations~~ information about gate ~~capacities~~ capacitances of said non-operating-state transistors in said non-operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state transistors and a power ~~are utilized to decide~~ terminal determines said equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

36. (currently amended) The method as claimed in claim 35, wherein a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating p-channel transistors in said non-operating state is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating n-channel transistors in said non-operating state is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

an arithmetic mean of a sum of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and a sum of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

an arithmetic mean of a sum of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and a sum of interconnection ~~capacities~~ capacitances between said non-operating n-channel transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

37. (currently amended) The method as claimed in claim 35, wherein a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel

transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

38. (currently amended) The method as claimed in claim 21, wherein, in said second sequential processes, ~~informations~~ information about an ~~averaged~~ average value of ON-resistances of all transistors included in said constituting gate circuits and the number of non-operating gate circuits ~~are utilized to decide~~ determine an ON-resistance of an equivalent internal ~~capacity ; and~~ capacitance;

~~informations~~ information about an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and the number of non-operating gate circuits as well as ~~informations~~ information about an ~~averaged~~ average value of interconnection capacitances between said operating-state transistors and a power ~~are utilized to decide~~ terminal determine said equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

39. (currently amended) The method as claimed in claim 38, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number

of said constituting logic gate included in said ~~semiconductor~~ integrated circuit and a remainder by subtracting an average operational rate from 1;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate ~~circuit~~ circuits is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel

transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

40. (currently amended) The method as claimed in claim 38, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said ~~semiconductor~~ integrated circuit and a remainder by subtracting a maximum operational rate from 1;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate ~~circuit~~ circuits is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate ~~circuit~~ circuits and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-

operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate ~~circuit~~ circuits and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

41. (currently amended) The method as claimed in claim 21, wherein ~~informations~~ information about an ~~averaged~~ average value of ON-resistances of all transistors included in said constituting gate circuits and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine an ON-resistance of an equivalent internal ~~capacity ; and~~ capacitance;

~~informations~~ information about an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits as well as

~~informations~~ information about an ~~averaged~~ average value of interconnection capacitances between said operating-state transistors and a power ~~are utilized to decide~~ terminal determine said equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

42. (currently amended) The method as claimed in claim 41, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of the total number of the constituting gate circuits included in the ~~semiconductor~~ integrated circuit and a power current ratio which is defined to be a ratio of an ~~averaged~~ average current value of all of basic gate circuits to an ~~averaged~~ average current value of all of the constituting gate circuits;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

43. (original) The method as claimed in claim 21, wherein said equivalent internal capacitive part is placed between said logic gate circuit part and a power system side.

44. (currently amended) The method as claimed in claim 21, wherein said power model ~~is deigned for simulation to~~ simulates a current distribution over a circuit board on which said ~~semiconductor~~ integrated circuit is mounted.

45. (currently amended) The method as claimed in claim 44, wherein said power model ~~is deigned for an~~ simulates electro-

magnetic interference ~~simulation to an electromagnetic field distribution~~ over a circuit board on which said ~~semiconductor~~ integrated circuit is mounted.

46. (currently amended) A storage medium [[for]] storing a computer program for designing a power model for ~~a semiconductor~~ an integrated circuit, and said power model comprising a logic gate circuit part and an equivalent internal capacitive part, the program comprising the step of:

~~wherein~~ performing first sequential processes to prepare said logic gate circuit part of said power model taking into account operating-related ~~informations~~ information of all gate circuits constituting said ~~semiconductor~~ integrated circuit ~~are utilized in first sequential processes to prepare said logic gate circuit part of said power model~~, and

~~wherein~~ performing second sequential processes separate from said first sequential processes to prepare said equivalent internal capacitive part of said power model taking into account non-operating-related ~~informations~~ information of said all gate circuits constituting said ~~semiconductor~~ integrated circuit ~~are utilized in second sequential processes separated from said first sequential processes to prepare said equivalent internal capacitive part of said power model~~.

47. (currently amended) The storage medium as claimed in claim 46, wherein, in said first sequential processes, ~~informations~~ information about gate widths of operating-state p-channel transistors in said operating-state of said constituting

gate circuits ~~are utilized to decide~~ determines a gate width of a model p-channel transistor;

~~informations~~ information about gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits ~~are utilized to decide~~ determines a gate width of a model n-channel transistor;

~~informations~~ information about gate ~~capacities~~ capacitances of said operating-state p-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state p-channel transistors and a first power ~~are utilized to decide~~ terminal determines a model first load ~~capacity~~ capacitance; [[and]]

~~informations~~ information about gate ~~capacities~~ capacitances of said operating-state n-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state n-channel transistors and a second power ~~are utilized to decide~~ terminal determines a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with at least a pair of p-channel and n-channel transistors and at least a pair of first and second load ~~capacities is designed~~ capacitances.

48. (currently amended) The storage medium as claimed in claim [[27]] 47, wherein a sum of gate widths of said

operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity; and~~ capacitance;

a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

49. (currently amended) The storage medium as claimed in claim 47, wherein a half of a sum of gate widths of said operating-state p-channel transistors in said operating-state of

said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity; and~~ capacitance;

a half of a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

50. (currently amended) The storage medium as claimed in claim 47, wherein a product of the number of said operating-state gate circuits and an ~~averaged~~ average value of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said operating-state gate circuits and an ~~averaged~~ average value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

51. (currently amended) The storage medium as claimed in claim 47, wherein a half of a product of the number of said

operating-state gate circuits and an ~~averaged~~ average value of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said operating-state gate circuits and an ~~averaged~~ average value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model

p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

52. (currently amended) The storage medium as claimed in claim 46, wherein, in said first sequential processes, ~~informations~~ information about gate widths of all p-channel transistors of said constituting gate circuits and [[an]] information about operational rate of operating-state p-channel transistors in said operating-state ~~are utilized to decide~~ determine a gate width of a model p-channel transistor;

~~informations~~ information about gate widths of all n-channel transistors of said constituting gate circuits and [[an]] information about operational rate of operating-state n-channel transistors in said operating-state ~~are utilized to decide~~ determine a gate width of a model n-channel transistor;

~~informations~~ information about gate ~~capacities~~ capacitances of said all p-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all p-channel transistors and a first power terminal and ~~informations~~ information about said operational rate ~~are utilized to decide~~ determine a model first load ~~capacity ; and~~ capacitance;

~~informations~~ information about gate ~~capacities~~ capacitances of said all n-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all n-channel transistors and a second power terminal and ~~informations~~

information about said operational rate ~~are utilized to decide~~ determine a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with at least a pair of said model p-channel and n-channel transistors and at least a pair of said model first and second load ~~capacities is designed~~ capacitances.

53. (currently amended) The storage medium as claimed in claim 52, wherein a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

54. (currently amended) The storage medium as claimed in claim 52, wherein a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and

a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

55. (currently amended) The storage medium as claimed in claim 52, wherein a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said

all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

56. (currently amended) The storage medium as claimed in claim 52, wherein a half of a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate

circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

57. (currently amended) The storage medium as claimed in claim 46, wherein, in said first sequential processes, ~~informations~~ information about gate widths of all p-channel transistors of said constituting gate circuits and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine a gate width of a model p-channel transistor;

~~informations~~ information about gate widths of all n-channel transistors of said constituting gate circuits and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine a gate width of a model n-channel transistor;

~~informations~~ information about gate ~~capacities~~ capacitances of said all p-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all p-channel transistors and a first power terminal and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine a model first load ~~capacity ; and~~ capacitance;

~~informations~~ information about gate ~~capacities~~ capacitances of said all n-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all n-channel transistors and a second power terminal and ~~informations~~ information about currents of basic gate circuits and said

constituting gate circuits ~~are utilized to decide~~ determine a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with at least a pair of p-channel and n-channel transistors and at least a pair of first and second load ~~capacities is designed~~ capacitances.

58. (currently amended) The storage medium as claimed in claim 57, wherein a product of the number of said all gate circuits, and a power current ratio of an ~~averaged~~ average current value of said basic gate circuits to an ~~averaged~~ average current value of said constituting gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said all gate circuits, said power current ratio, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

59. (currently amended) The storage medium as claimed in claim 57, wherein a half of a product of the number of said all gate circuits, and a power current ratio of an ~~averaged~~ average current value of said basic gate circuits to an ~~averaged~~ average current value of said constituting gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said all gate circuits, said power current ratio, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

60. (currently amended) The storage medium as claimed in claim 46, wherein, in said second sequential processes, ~~informations~~ information about ON-resistances of non-operating-state, transistors in said non-operating-state of said constituting gate circuits ~~are utilized to decide~~ determines an ON-resistance of an equivalent internal ~~capacity ; and~~ capacitance;

~~informations~~ information about gate ~~capacities~~ capacitances of said non-operating-state transistors in said non-operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state transistors and a power ~~are utilized to decide~~ terminal determines said equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

61. (currently amended) The storage medium as claimed in claim 60, wherein a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating p-channel transistors in said non-operating state is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating n-channel transistors in said non-operating state is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

an arithmetic mean of a sum of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and a sum of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

an arithmetic mean of a sum of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and a

sum of interconnection ~~capacities~~ capacitances between said non-operating n-channel transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

62. (currently amended) The storage medium as claimed in claim 60, wherein a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

63. (currently amended) The storage medium as claimed in claim 46, wherein, in said second sequential processes, ~~informations~~ information about an ~~averaged~~ average value of ON-resistances of all transistors included in said constituting gate circuits and the number of non-operating gate circuits ~~are utilized to decide~~ determine an ON-resistance of an equivalent internal ~~capacity ; and~~ capacitance;

~~informations~~ information about an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and the number of non-operating gate circuits as well as ~~informations~~ information about an ~~averaged~~ average value of interconnection capacitances between said operating-state transistors and a power ~~are utilized to decide~~ terminal determine said equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

64. (currently amended) The storage medium as claimed in claim 63, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said ~~semiconductor~~ integrated circuit and a remainder by subtracting an average operational rate from 1;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate ~~circuit~~ circuits is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

65. (currently amended) The storage medium as claimed in claim 63, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said ~~semiconductor~~ integrated circuit and a remainder by subtracting a maximum operational rate from 1;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate ~~circuit~~ circuits is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate ~~circuit~~ circuits and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate ~~circuit~~ circuits and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

66. (currently amended) The storage medium as claimed in claim 46, wherein ~~informations~~ information about an ~~averaged~~ average value of ON-resistances of all transistors included in said constituting gate circuits and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine an ON-resistance of an equivalent internal ~~capacity ; and~~ capacitance;

~~informations~~ information about an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits as well as ~~informations~~ information about an ~~averaged~~ average value of interconnection capacitances between said operating-state transistors and a power ~~are utilized to decide~~ terminal determine said equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

67. (currently amended) The storage medium as claimed in claim 66, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of the total number of the constituting gate circuits included in the ~~semiconductor~~ integrated circuit and a power current ratio which is defined to be a ratio of an ~~averaged~~ average current value of all of basic gate circuits to an ~~averaged~~ average current value of all of the constituting gate circuits;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

68. (original) The storage medium as claimed in claim 46, wherein said equivalent internal capacitive part is placed between said logic gate circuit part and a power system side.

69. (currently amended) The storage medium as claimed in claim 46, wherein said power model ~~is deigned for simulation to~~ simulates a current distribution over a circuit board on which said ~~semiconductor~~ integrated circuit is mounted.

70. (currently amended) The storage medium as claimed in claim 69, wherein said power model ~~is deigned for an~~ simulates electro-magnetic interference ~~simulation to an electromagnetic field distribution~~ over a circuit board on which said ~~semiconductor~~ integrated circuit is mounted.

71. (currently amended) A supporting system for designing a power model for ~~a semiconductor~~ an integrated circuit, ~~and said~~ the power model ~~comprising~~ including a logic gate circuit part and an equivalent internal capacitive part, [[and]] said supporting system comprising:

a data base storing ~~informations of~~ integrated circuit internal circuit ~~configurations ;~~ configuration information;

a storage medium [[for]] storing ~~informations~~ information about circuit elements and interconnections between said circuit elements of said power model as well as [[for]] storing a computer program for designing said power model;

a processor ~~being~~ connected to said data base and said storage medium for executing said computer program to prepare said power model; and

an output device ~~being~~ connected to said processor for outputting said power model prepared by said processor, said computer program comprising the steps of:

~~wherein~~ performing first sequential processes to prepare said logic gate circuit part of said power model taking into account operating-related ~~informations~~ information of all gate circuits constituting said ~~semiconductor~~ integrated circuit ~~are utilized in first sequential processes to prepare said logic gate circuit part of said power model~~, and

~~wherein~~ performing second sequential processes separate from said first sequential processes to prepare said equivalent internal capacitive part of said power model taking into account non-operating-related ~~informations~~ information of said all gate circuits constituting said ~~semiconductor~~ integrated circuit ~~are utilized in second sequential processes separated from said first sequential processes to prepare said equivalent internal capacitive part of said power model~~.

72. (currently amended) The supporting system as claimed in claim 71, wherein, in said first sequential processes, ~~informations~~ information about gate widths of operating-state p-channel transistors in said operating-state of said constituting gate circuits ~~are utilized to decide~~ determines a gate width of a model p-channel transistor;

~~informations~~ information about gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits ~~are utilized to decide~~ determines a gate width of a model n-channel transistor;

~~informations~~ information about gate ~~capacities~~ capacitances of said operating-state p-channel transistors in

said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state p-channel transistors and a first power ~~are utilized to decide~~ terminal determines a model first load ~~capacity~~ capacitance; [[and]]

~~informations~~ information about gate ~~capacities~~ capacitances of said operating-state n-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state n-channel transistors and a second power ~~are utilized to decide~~ terminal determines a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with at least a pair of p-channel and n-channel transistors and at least a pair of first and second load ~~capacities is designed~~ capacitances.

73. (currently amended) The supporting system as claimed in claim [[52]] 72, wherein a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity; and~~ capacitance;

a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

74. (currently amended) The supporting system as claimed in claim 72, wherein a half of a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances

between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity; and~~ capacitance;

a half of a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

75. (currently amended) The supporting system as claimed in claim 72, wherein a product of the number of said operating-state gate circuits and an ~~averaged~~ average value of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said operating-state gate circuits and an ~~averaged~~ average value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state p-channel transistors and a

second ~~averaged~~ average value of interconnection capacitances between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

76. (currently amended) The supporting system medium as claimed in claim 72, wherein a half of a product of the number of said operating-state gate circuits and an ~~averaged~~ average value of gate widths of said operating-state p-channel transistors, in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said operating-state gate circuits and an ~~averaged~~ average value of gate widths of operating-state n-channel transistors in said operating-state

of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said operating-state p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said operating-state gate circuits and a sum of both a first ~~averaged~~ average value of gate capacitances of said operating-state n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said operating-state n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

77. (currently amended) The supporting system as claimed in claim 71, wherein, in said first sequential processes, ~~informations~~ information about gate widths of all p-channel transistors of said constituting gate circuits and [[an]] information about operational rate of operating-state p-channel

transistors in said operating-state ~~are utilized to decide~~ determine a gate width of a model p-channel transistor;

~~informations~~ information about gate widths of all n-channel transistors of said constituting gate circuits and [[an]] information about operational rate of operating-state n-channel transistors in said operating-state ~~are utilized to decide~~ determine a gate width of a model n-channel transistor;

~~informations~~ information about gate ~~capacities~~ capacitances of said all p-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all p-channel transistors and a first power terminal and ~~informations~~ information about said operational rate ~~are utilized to decide~~ determine a model first load ~~capacity ; and~~ capacitance;

~~informations~~ information about gate ~~capacities~~ capacitances of said all n-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all n-channel transistors and a second power terminal and ~~informations~~ information about said operational rate ~~are utilized to decide~~ determine a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with at least a pair of said model p-channel and n-channel transistors and at least a pair of said model first and second load ~~capacities is designed~~ capacitances.

78. (currently amended) The supporting system as claimed in claim 77, wherein a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

79. (currently amended) The supporting system as claimed in claim 77, wherein a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and

a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

80. (currently amended) The supporting system as claimed in claim 77, wherein a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel

transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

81. (currently amended) The supporting system as claimed in claim 77, wherein a half of a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

82. (currently amended) The supporting system as claimed in claim 71, wherein, in said first sequential processes, ~~informations~~ information about gate widths of all p-channel transistors of said constituting gate circuits and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine a gate width of a model p-channel transistor;

~~informations~~ information about gate widths of all n-channel transistors of said constituting gate circuits and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine a gate width of a model n-channel transistor;

~~informations~~ information about gate ~~capacities~~ capacitances of said all p-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all p-channel transistors and a first power terminal and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine a model first load ~~capacity ; and~~ capacitance;

~~informations~~ information about gate ~~capacities~~ capacitances of said all n-channel transistors of said constituting gate circuits and ~~informations~~ information about interconnection capacitances between said all n-channel transistors and a second power terminal and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with at least a pair of p-channel and n-channel transistors and at least a pair of first and second load ~~capacities is designed~~ capacitances.

83. (currently amended) The supporting system as claimed in claim 82, wherein a product of the number of said all gate circuits, and a power current ratio of an ~~averaged~~ average current value of said basic gate circuits to an ~~averaged~~ average current value of said constituting gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a product of the number of said all gate circuits, said power current ratio, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power

terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with a single pair of said model p-channel and n-channel transistors and a single pair of said model first and second load ~~capacities is designed~~ capacitances.

84. (currently amended) The supporting system as claimed in claim 82, wherein a half of a product of the number of said all gate circuits, and a power current ratio of an ~~averaged~~ average current value of said basic gate circuits to an ~~averaged~~ average current value of said constituting gate circuits, and an ~~averaged~~ average value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor;

a half of a product of the number of said all gate circuits, said power current ratio, and an ~~averaged~~ average value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor;

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all p-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all p-channel

transistors and said first power terminal is defined to be a model first load ~~capacity ; and~~ capacitance;

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first ~~averaged~~ average value of gate capacitances of said all n-channel transistors and a second ~~averaged~~ average value of interconnection capacitances between said all n-channel transistors and said second power terminal is defined to be a model second load ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said logic gate circuit part ~~comprising~~ with two pairs of said model p-channel and n-channel transistors and two pairs of said model first and second load ~~capacities is designed~~ capacitances.

85. (currently amended) The supporting system as claimed in claim 71, wherein, in said second sequential processes, ~~informations~~ information about ON-resistances of non-operating-state transistors in said non-operating-state of said constituting gate circuits ~~are utilized to decide~~ determines an ON-resistance of an equivalent internal ~~capacity ; and~~ capacitance;

~~informations~~ information about gate ~~capacities~~ capacitances of said non-operating-state transistors in said non-operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state transistors and a power ~~are utilized to decide~~ terminal determines said equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

86. (currently amended) The supporting system as claimed in claim 85, wherein a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating p-channel transistors in said non-operating state is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating n-channel transistors in said non-operating state is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

an arithmetic mean of a sum of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and a sum of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

an arithmetic mean of a sum of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and a sum of interconnection ~~capacities~~ capacitances between said non-operating n-channel transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

87. (currently amended) The supporting system as claimed in claim 85, wherein a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel

transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

88. (currently amended) The supporting system as claimed in claim 71, wherein, in said second sequential processes, ~~informations~~ information about an ~~averaged~~ average value of ON-resistances of all transistors included in said constituting gate circuits and the number of non-operating gate circuits ~~are utilized to decide~~ determine an ON-resistance of an equivalent internal ~~capacity ; and~~ capacitance;

~~informations~~ information about an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and the number of non-operating gate circuits as well as ~~informations~~ information about an ~~averaged~~ average value of interconnection capacitances between said operating-state transistors and a power ~~are utilized to decide~~ terminal determine said equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

89. (currently amended) The supporting system as claimed in claim 88, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product

of a total number of said constituting logic gate included in said ~~semiconductor~~ integrated circuit and a remainder by subtracting an average operational rate from 1;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate ~~circuit~~ circuits is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel

transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

90. (currently amended) The supporting system as claimed in claim 88, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said ~~semiconductor~~ integrated circuit and a remainder by subtracting a maximum operational rate from 1;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate ~~circuit~~ circuits is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate ~~circuit~~ circuits and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-

operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate ~~circuit~~ circuits and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

91. (currently amended) The supporting system as claimed in claim 71, wherein ~~informations~~ information about an ~~averaged~~ average value of ON-resistances of all transistors included in said constituting gate circuits and ~~informations~~ information about currents of basic gate circuits and said constituting gate circuits ~~are utilized to decide~~ determine an ON-resistance of an equivalent internal ~~capacity ; and~~ capacitance;

~~informations~~ information about an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and ~~informations~~ information about currents of basic

gate circuits and said constituting gate circuits as well as ~~informations~~ information about an ~~averaged~~ average value of interconnection capacitances between said operating-state transistors and a power ~~are utilized to decide~~ terminal determine said equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

92. (currently amended) The supporting system as claimed in claim 91, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of the total number of the constituting gate circuits included in the ~~semiconductor~~ integrated circuit and a power current ratio which is defined to be a ratio of an ~~averaged~~ average current value of all of basic gate circuits to an ~~averaged~~ average current value of all of the constituting gate circuits;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal ~~capacity ;~~ capacitance;

a double of a product of an ~~averaged~~ average value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal ~~capacity ;~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating p-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating p-channel transistors and a first power terminal is defined to be said second equivalent internal ~~capacity ; and~~ capacitance;

a product of said number of said non-operating gate circuit and an arithmetic mean of an ~~averaged~~ average value of gate ~~capacities~~ capacitances of said non-operating n-channel transistors and an ~~averaged~~ average value of interconnection ~~capacities~~ capacitances between said non-operating n-channel transistors and a second power terminal is defined to be said third equivalent internal ~~capacity,~~ capacitance; and

~~whereby~~ further comprising the step of designing said equivalent internal capacitive part ~~comprising~~ with at least said equivalent internal ~~capacity is designed~~ capacitance.

93. (original) The supporting system as claimed in claim 71, wherein said equivalent internal capacitive part is placed between said logic gate circuit part and a power system side.

94. (currently amended) The supporting system as claimed in claim 71, wherein said power model ~~is deigned for simulation to~~ simulates a current distribution over a circuit board on which said ~~semiconductor~~ integrated circuit is mounted.

95. (currently amended) The supporting system as claimed in claim 94, wherein said power model ~~is deigned for an~~ simulates electro-magnetic interference ~~simulation to an electromagnetic field distribution~~ over a circuit board on which said ~~semiconductor~~ integrated circuit is mounted.

96. (currently amended) The supporting system as claimed in claim 71, wherein said computer program further includes a first simulation program for ~~analysis to~~ analyzing circuits.

97. (currently amended) The supporting system as claimed in claim 96, wherein said first simulation program ~~is to obtain~~ obtains a current distribution over a circuit board on which said semiconductor integrated circuit is mounted.

98. (currently amended) The supporting system as claimed in claim 97, wherein said computer program further [[more]] includes a second simulation program for ~~analysis to~~ analyzing an electromagnetic field to obtain a distribution of the electromagnetic field over said circuit board on which said ~~semiconductor~~ integrated circuit is mounted.

99. (currently amended) A simulator for simulating an electro-magnetic interference, said simulator comprising:

a circuit analyzing simulator ~~being accessible to~~ that accesses a first storage medium ~~for receiving~~ storing a power model for ~~a semiconductor~~ an integrated circuit, and ~~also being connected to~~ accessing a second storage medium ~~for receiving informations~~ storing information about a circuit board on which

said ~~semiconductor~~ integrated circuit is mounted, so that said circuit analyzing simulator analyzes said power model to obtain a current distribution over [[a]] said circuit board ~~on which said semiconductor integrated circuit is mounted~~;

an electromagnetic field analyzing simulator ~~being accessible to~~ that accesses said circuit analyzing simulator ~~for receiving~~ and receives said current distribution[[,]] so that said electromagnetic field analyzing simulator analyzes an electromagnetic field distribution over said circuit board ~~on which said semiconductor integrated circuit is mounted,~~; and

~~wherein~~ said power model ~~comprises~~ comprising a logic gate circuit part representing an operating part of said ~~semiconductor~~ integrated circuit and an equivalent internal capacitive part representing a non-operating part of said ~~semiconductor~~ integrated circuit.

100. (currently amended) The simulator as claimed in claim 99, wherein said power model is independently provided for each of plural power systems which are independent from each other and included in said ~~semiconductor~~ integrated circuit.

101. (currently amended) The simulator as claimed in claim 99, wherein an internal circuit ~~configurations~~ configuration of said ~~semiconductor~~ integrated circuit ~~are~~ is divided into plural blocks on the basis of arrangement ~~informations~~ information, and a separate said power model is provided for each of said plural blocks.

102. (currently amended) The simulator as claimed in claim 99, wherein an internal circuit ~~configurations~~ configuration of said semiconductor integrated circuit ~~are~~ is divided into plural groups, wherein each of said plural groups comprises ~~a same timing group which includes~~ logic gate circuits having ~~individual~~ signal transmission delay times ~~fallen~~ in a ~~group-belonging~~ predetermined time range which ~~belongs to~~ is different for each of said plural groups, and wherein a separate said power model is provided for each of said plural groups.

103. (currently amended) The simulator as claimed in claim 99, wherein said power model further comprises a signal source connected to said logic gate circuit part for supplying a frequency-fixed signal to said logic gate circuit part, so that said logic gate circuit part represents operating state parts of said ~~semiconductor~~ integrated circuit in accordance with said frequency-fixed signal, and said equivalent internal capacitive part represents non-operating state parts of said ~~semiconductor~~ integrated circuit.

104. (currently amended) The simulator as claimed in claim 103, wherein said equivalent internal capacitive part further represents operating-irrelevant fixed parts of said ~~semiconductor~~ integrated circuit.

105. (currently amended) The simulator as claimed in claim 104, wherein said logic gate circuit part is connected between first and second ~~powers~~ power terminals, and said

equivalent internal capacitive part is also connected between said first and second ~~powers~~ power terminals.

106. (currently amended) The simulator as claimed in claim 105, wherein said logic gate circuit part further comprises a single pair of an inverter circuit and a load capacitive element, and said inverter circuit is connected between said first and second ~~powers~~ power terminals and said load capacitive element is also connected between said first and second ~~powers~~ power terminals, and said load capacitive element is placed between said inverter circuit and said equivalent internal capacitive part.

107. (currently amended) The simulator as claimed in claim 106, wherein said load capacitive element comprises a series connection of a first load capacitance and a second load capacitance between said first and second ~~powers~~ power terminals, and an intermediate point between said first and second load capacitances is connected to an output terminal of said inverter circuit.

108. (currently amended) The simulator as claimed in claim 107, wherein said equivalent internal capacitive part further comprises at least an equivalent internal capacitive element connected between said first and second ~~powers~~ power terminals.

109. (currently amended) The simulator as claimed in claim 108, wherein a plurality of said equivalent internal capacitive element is connected between said first and second

~~powers~~ power terminals, and said equivalent internal capacitive element comprises a series connection of a capacitance and a resistance between said first and second ~~powers~~ power terminals.

110. (original) The simulator as claimed in claim 109, wherein said inverter circuit comprises a series connection of a p-channel MOS field effect transistor and an n-channel MOS field effect transistor, and gate electrodes of said p-channel and n-channel MOS field effect transistors are connected to a clock signal source for applying a clock signal to said gate electrodes of said p-channel and n-channel MOS field effect transistors.

111. (currently amended) The simulator as claimed in claim 105, wherein said logic gate circuit part further comprises plural pairs of an inverter circuit and a load capacitive element, and said inverter circuit is connected between said first and second ~~powers~~ power terminals and said load capacitive element is also connected between said first and second ~~powers~~ power terminals, and in each pair, said load capacitive element is placed closer to said equivalent internal capacitive part than said inverter circuit.

112. (currently amended) The simulator as claimed in claim 111, wherein said load capacitive element comprises a series connection of a first load capacitance and a second load capacitance between said first and second ~~powers~~ power terminals, and an intermediate point between said first and second load capacitances is connected to an output terminal of said inverter circuit.

113. (currently amended) The simulator as claimed in claim 112, wherein said equivalent internal capacitive part further comprises at least an equivalent internal capacitive element connected between said first and second ~~powers~~ power terminals.

114. (currently amended) The simulator as claimed in claim 113, wherein a plurality of said equivalent internal capacitive element is connected between said first and second ~~powers~~ power terminals, and said equivalent internal capacitive element comprises a series connection of a capacitance and a resistance between said first and second ~~powers~~ power terminals.

115. (original) The simulator as claimed in claim 114, wherein said inverter circuit comprises a series connection of a p-channel MOS field effect transistor and an n-channel MOS field effect transistor, and gate electrodes of said p-channel and n-channel MOS field effect transistors are connected to a clock signal source for applying a clock signal to said gate electrodes of said p-channel and n-channel MOS field effect transistors.

116. (original) The simulator as claimed in claim 99, wherein said equivalent internal capacitive part is placed between said logic gate circuit part and a power system side.